

FIG. 1
PRIOR ART

The diagram shows a differential signal processing circuit. It consists of a first differential pair (transistors 1 and 2) with sources connected to a common source node (XTN) and gates biased by BIASP and BIASP. This pair is followed by a second differential pair (transistors 3 and 4) with sources connected to ground (VSS) and gates biased by BIASN and BIASN. A feedback loop is formed by a third differential pair (transistors 5 and 6) whose gates are biased by BIASN and BIASN, and whose sources are connected to the gates of the first pair. The outputs of the first pair (OUTP, OUTN) are connected to the gates of the third pair. A dashed box labeled D1 encloses the first and second differential pairs, and a dashed box labeled D2 encloses the third differential pair. A dashed box labeled A encloses the third differential pair and its feedback connections. The circuit is powered by VDD and VSS, with common mode nodes CM1 and CM2 indicated.

FIG. 2

FIG. 3A

FIG. 3A

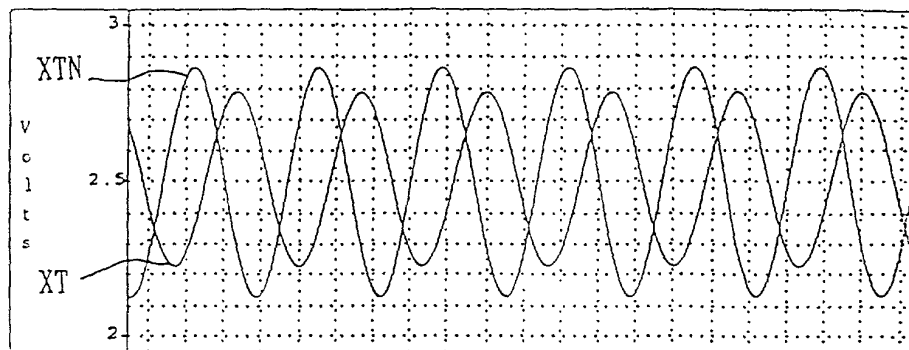


FIG. 3B

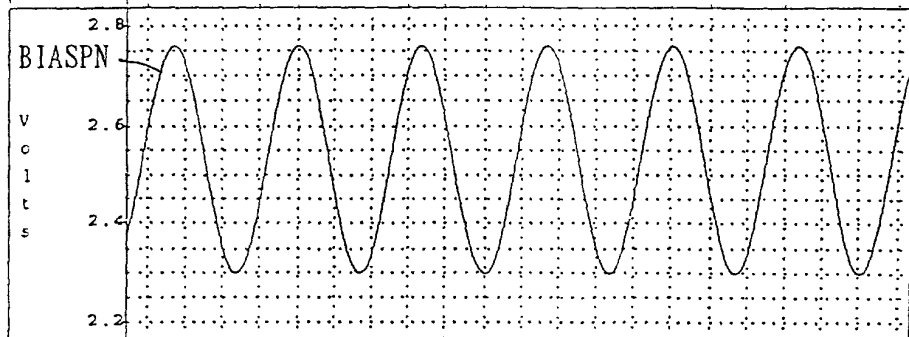


FIG. 3C

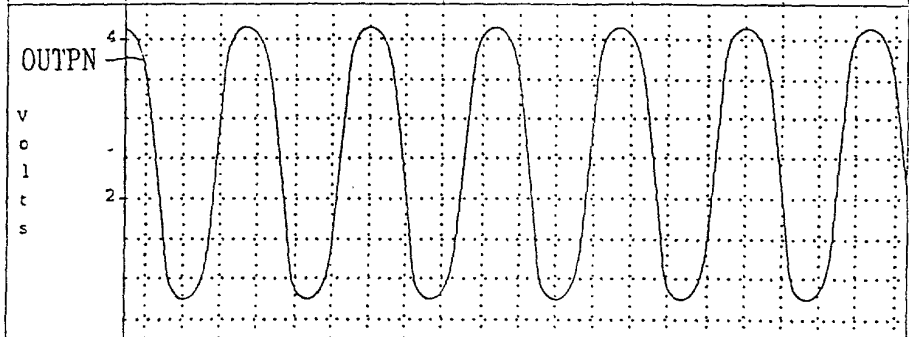
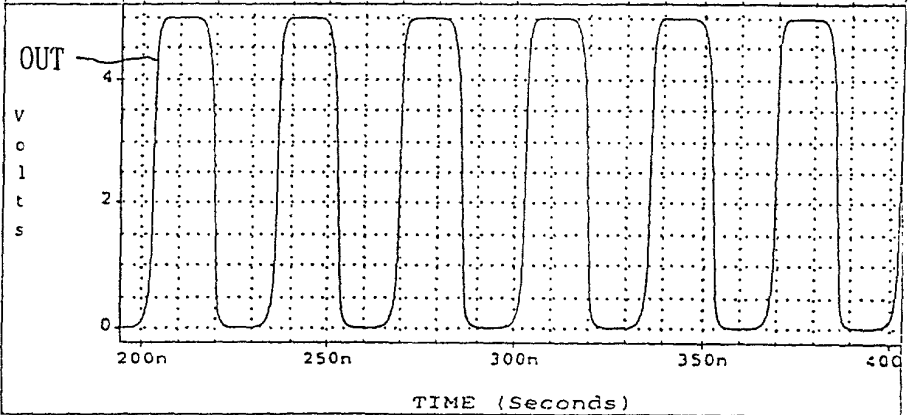


FIG. 3D



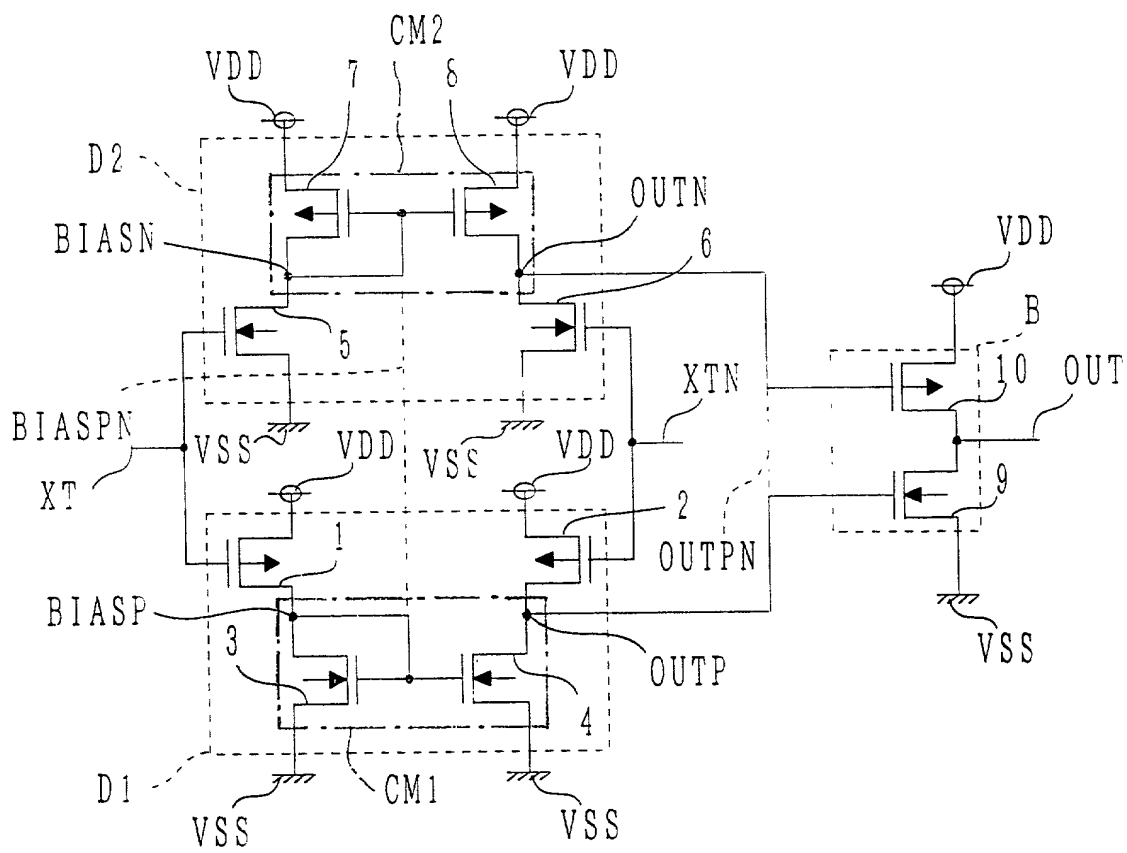


FIG. 4

FIG. 5A

FIG. 5A

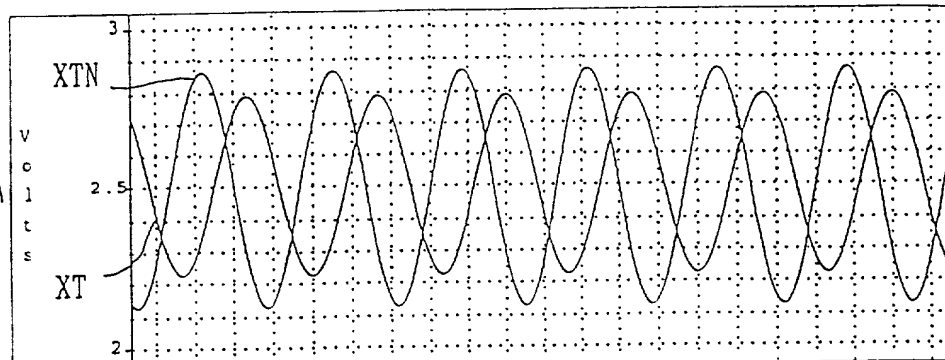


FIG. 5B

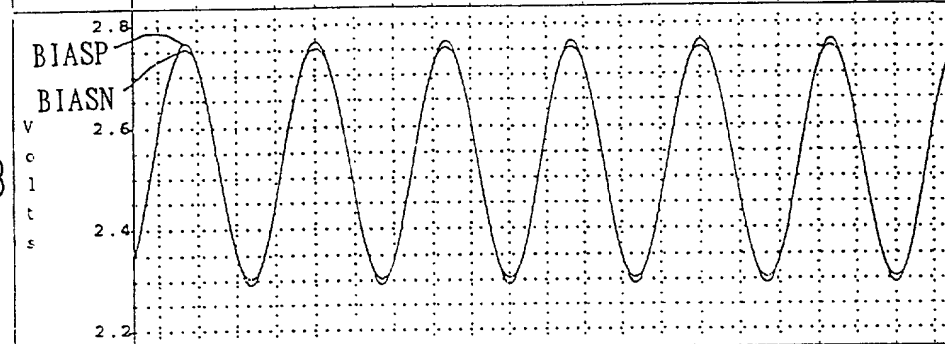


FIG. 5C

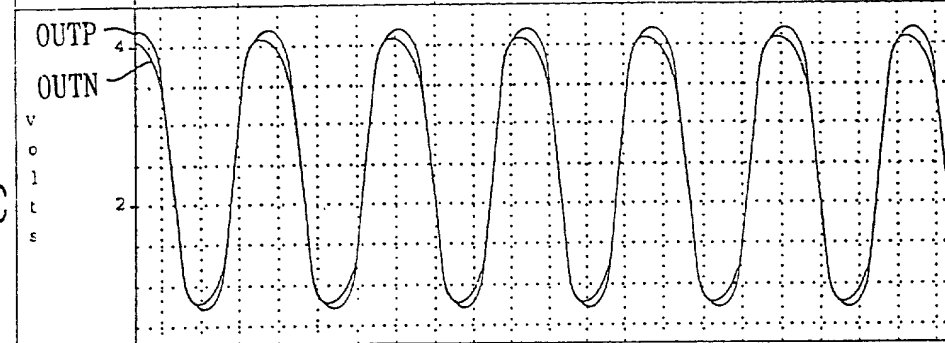
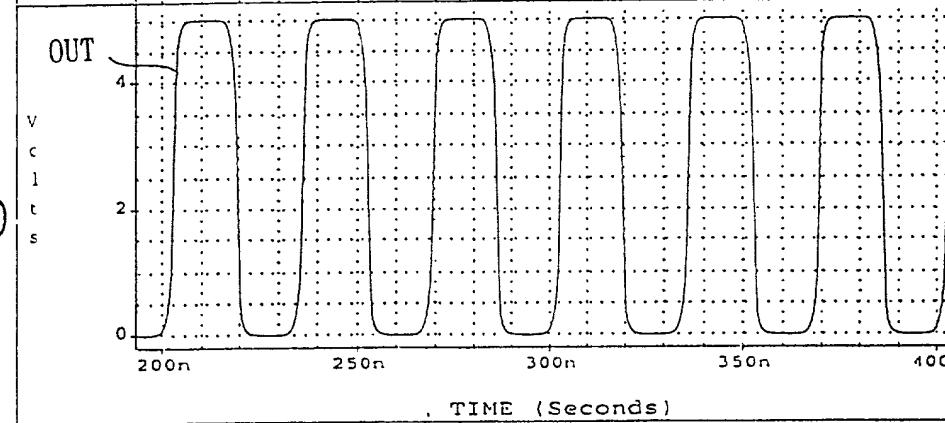


FIG. 5D



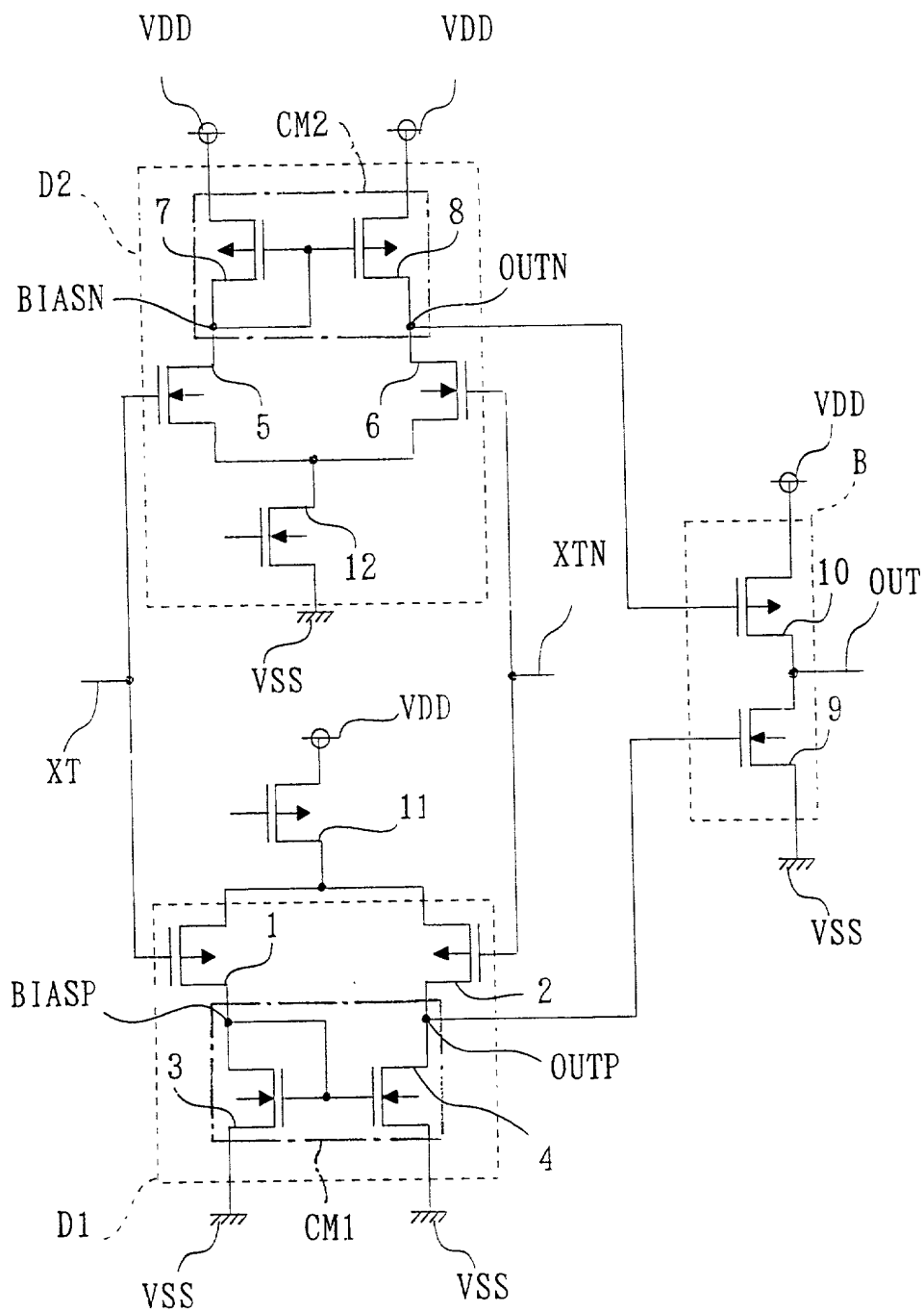


FIG. 6

FIG. 7A

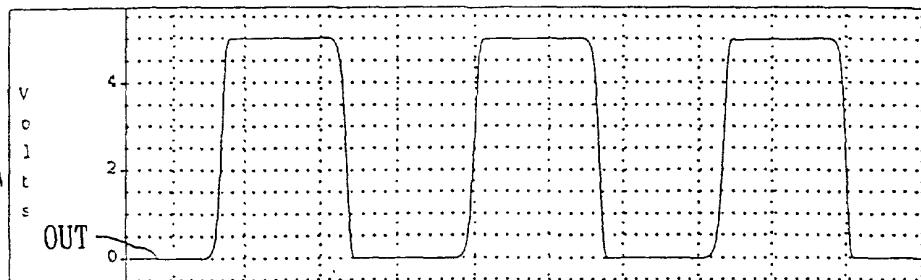


FIG. 7B

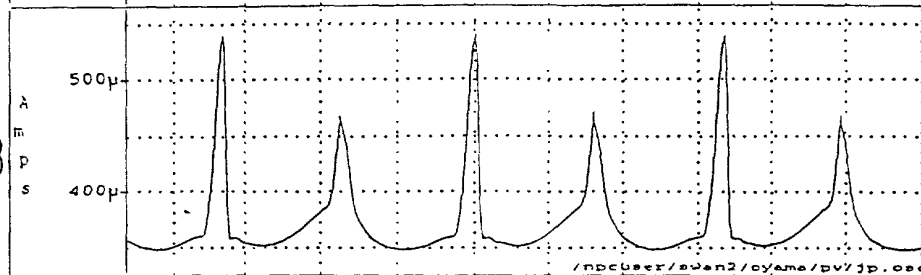


FIG. 7C

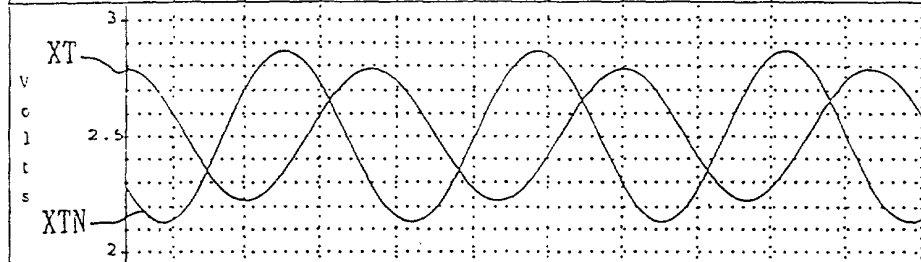


FIG. 7D

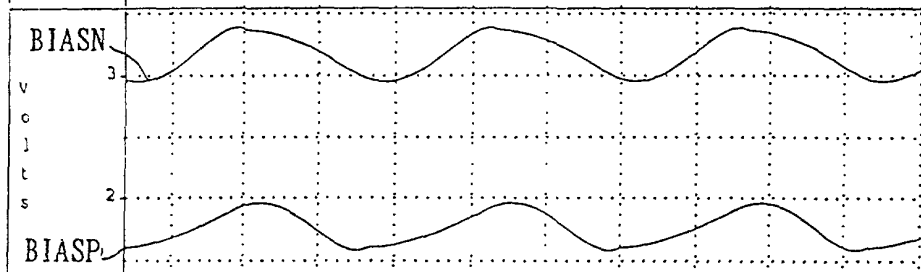


FIG. 7E

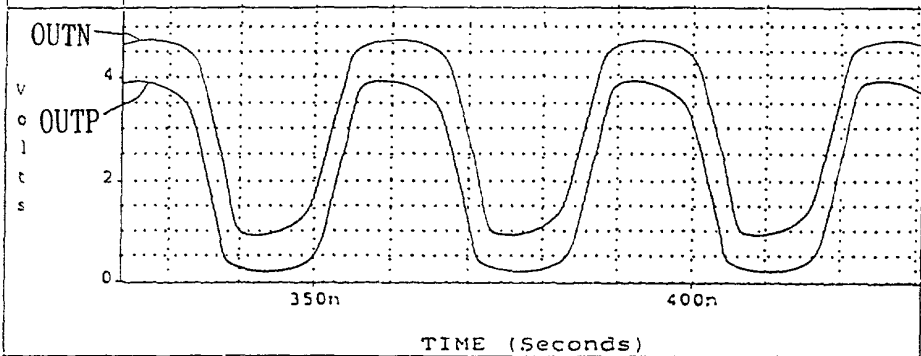


FIG. 8A

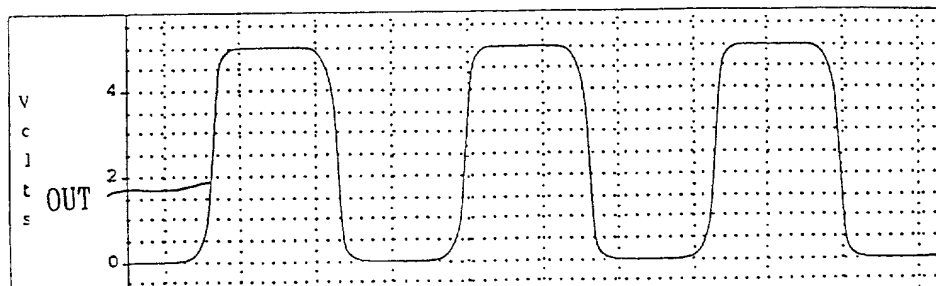


FIG. 8B

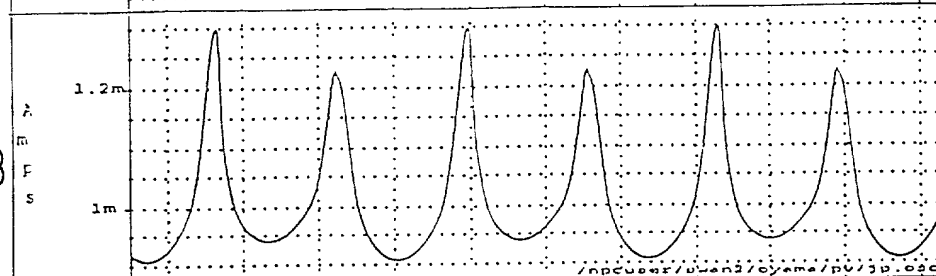


FIG. 8C

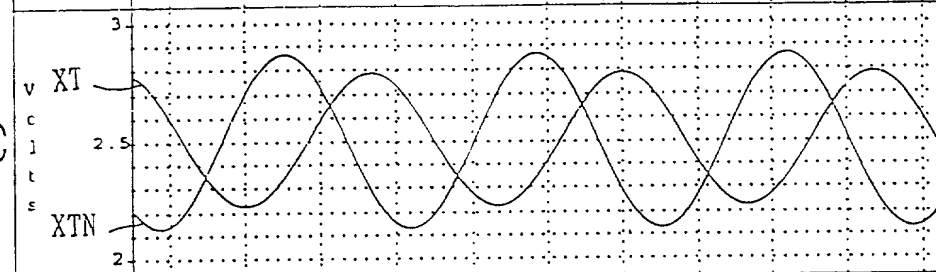


FIG. 8D

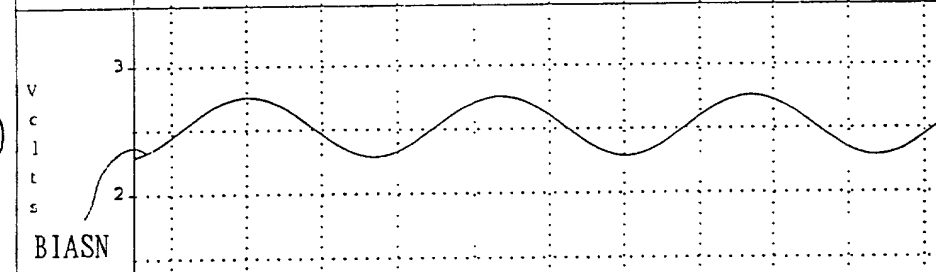
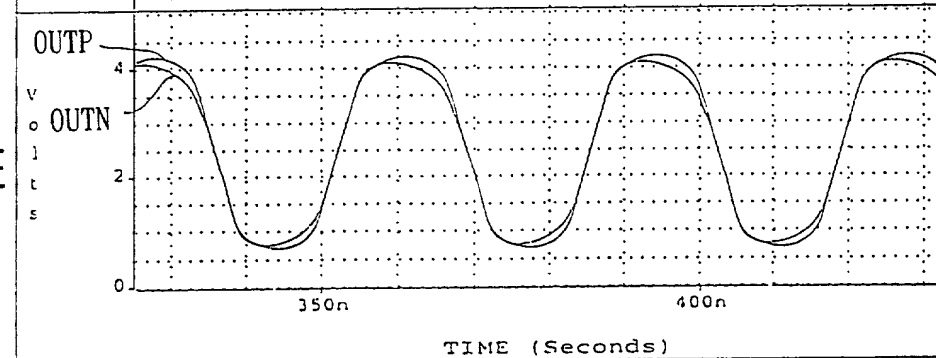


FIG. 8E



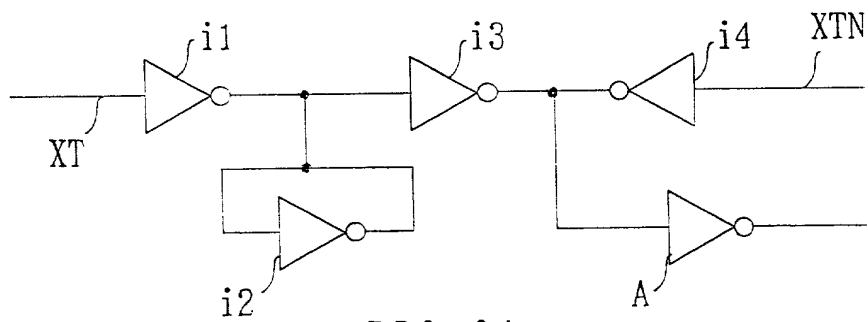


FIG. 9A

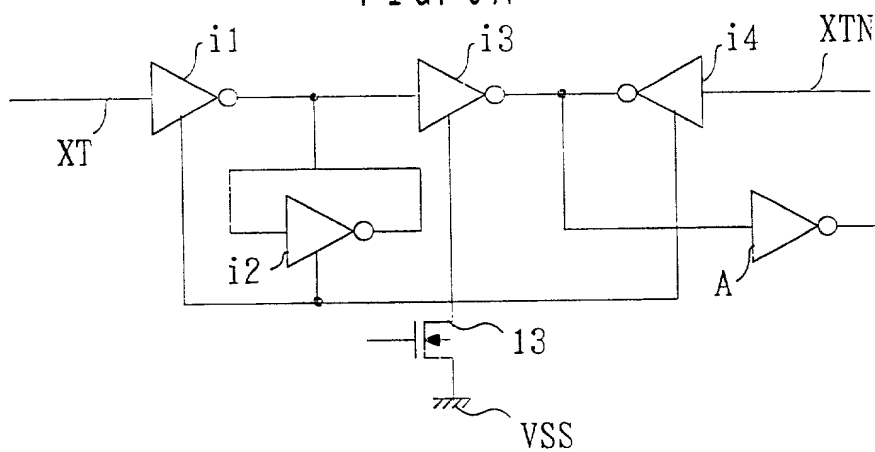


FIG. 9B

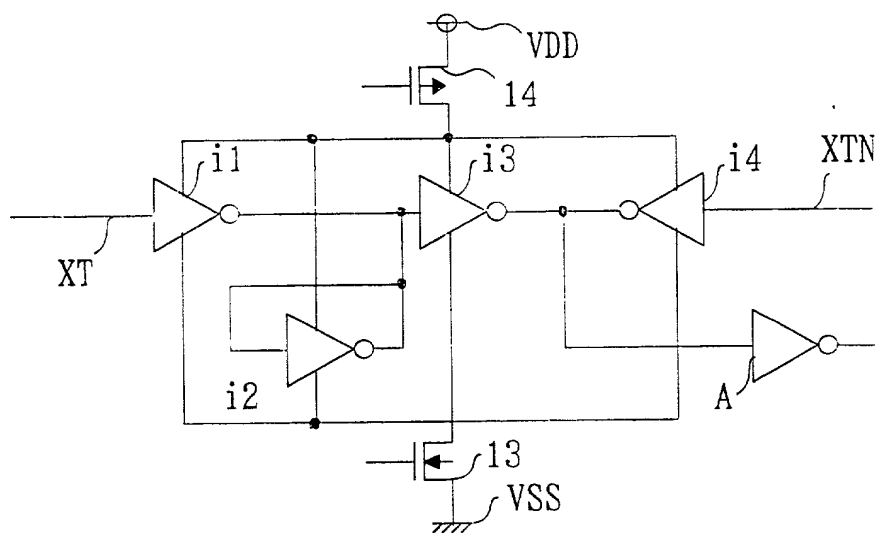


FIG. 9C